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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,056	09/05/2003	WEI-CHUN KUNG	9388-US-PA	2055
31561	7590	03/16/2005	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			BEREZNY, NEMA O	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/605,056

Applicant(s)

KUNG ET AL.

Examiner

Nema O. Berezny

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date: \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of claims 1-13 in the reply filed on 12-28-04 is acknowledged. Cancellation of claims 14-31 is also acknowledged.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5, 10, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita (5,509,203). Yamashita discloses a packaging process, comprising the steps of: providing an insulation layer (Figs.7A-8 el.2), wherein the insulation layer has an upper surface and a corresponding lower surface; forming a plurality of openings (el.6) passing through the insulation layer; attaching a tape (el.10) onto the lower surface of the insulation layer; forming a conductive body (el.8, 4a) inside the openings; mounting a chip (el.12) over the upper surface of the insulation layer and the chip electrically connected with the conductive body (Fig.8); and removing the tape (Fig.7E-7F; col.5 lines 46-48) [**claim 1**]. Yamashita also discloses wherein forming the conductive body inside the openings comprises electroless plating (col.6 lines 39-42, wherein electroless plating is implied from cited different embodiment) [**claim 2**];

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wherein mounting the chip over the upper surface of the insulation layer comprises mounting the chip over the upper surface of the insulation layer via a plurality of bumps (el.12a), the bumps electrically connecting the conductive body with the chip **[claim 5]**; wherein material constituting the conductive body includes gold (col.5 lines 19-21) **[claim 10]**; and wherein material constituting the insulation layer is selected from a group consisting of glass epoxy resin, Bismaleimide-Triazine, polyimide and epoxy resin (col.6 lines 15-22) **[claim 13]**.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita as applied to claim 1 above, and further in view of Lin et al. (5,200,362). Yamashita discloses a chip with an active surface, a corresponding backside and a plurality of chip contacts (Fig.8 no #) on the active surface. However, Yamashita does not disclose a die pad. Yamashita would look to one such as Lin for a face-up chip mounting because Lin discloses wherein the conductive body has a die pad (Fig.2 el.13) and a plurality of contacts (el.13). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the die pad of Lin with the process of Yamashita in order to also mount a chip to a substrate in the face-up

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position **[claim 3]**. Based upon the rejection of claim 3 above, Lin also discloses wherein mounting the chip over the upper surface of the insulation layer comprises attaching the backside of the chip onto the die pad (Fig.2), electrically connecting the chip contacts with the contacts of the conductive body via a plurality of conductive wires (el.18), and forming a packaging material (el.20) to encapsulate the chip and the conductive wires (Fig.3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the mounting and encapsulating of Lin with the process of Yamashita in order to protect the chip (col.3 lines 13-17) **[claim 4]**.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita as applied to claims 1 and 5 above, and further in view of Wang et al. (5,817,545). Yamashita does not disclose an insulation material between the chip and insulation layer. However, Yamashita would look to one such as Wang for protection because Wang discloses wherein after mounting the chip over the insulation layer through the bumps, an insulation material (Fig.2 el.23) is filled into the space between the chip (el.20) and the insulation layer (el.21) and the bumps (el.22) are enclosed by the insulation material. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the insulation material of Wang with the process of Yamashita in order to protect the device, wherein the encapsulant can be made of reworkable material (abstract).

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita as applied to claim 1 above, and further in view of Ino (2002/0142520). Yamashita does not disclose a multi-layer substrate. However, Yamashita would look to one such as Ino for forming a base layer and an adherent layer separately because Ino discloses wherein before mounting the chip over the upper surface of the insulation layer, a multi-layer substrate is formed by further conducting the steps comprising: forming an additional insulation layer (Fig.4b el.2) over the insulation layer (el.1); forming a plurality of openings (el.4b) passing through the additional insulation layer; and forming an additional conductive body (el.4) inside the openings of the additional insulation layer (p.2 para.34). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the multi-layer substrate of Ino with the process of Yamashita in order to form the base substrate from reel material with the adherent added later (p.2 para.31,32).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita as applied to claim 1 above, and further in view of Grupen-Shemansky et al. (6,022,761). Yamashita does not disclose a copper conductive body. However, Yamashita would look to one such as Grupen-Shemansky for solderability because Grupen-Shemansky discloses wherein material constituting the conductive body includes copper (Fig.3; col.4 lines 3-7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the copper conductive material of Grupen-Shemansky with the process of Yamashita in order to

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provide solderable metal that will easily bond or connect to another substrate (Fig.3; col.4 lines 3-7).

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita as applied to claim 1 above, and further in view of Hsieh et al. (2003/0022477). Yamashita does not disclose multiple metallic layers. However, Yamashita would look to one such as Hsieh for forming a barrier layer because Hsieh discloses wherein the conductive body is a composite structure comprising multiple metallic layers, and wherein the conductive body is a composite structure comprising a gold layer, a palladium layer, a nickel layer and a palladium layer (p.2 para.25). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the multiple metallic layers of Hsieh with the process of Yamashita in order to form a barrier layer (p.2 para.25).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O. Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

  
**ERIK KIELIN**  
**PRIMARY EXAMINER**